PEREGRINE SEMICONDUCTOR

AN16: Application Note

Using Peregrine Phase-Locked Loop Integrated Circuits in Reference and System Clock Applications

Features

- Very Low Phase Noise
  - 0.07° RMS Jitter at 155 MHz
  - 0.18° RMS Jitter at 1.8 GHz
- No Microcontroller Required

Summary

High-speed communications and measurement systems require low jitter system clocks or references. This Application Note shows several examples of how Peregrine Integer-N PLL devices can be used to create extremely low jitter high frequency clocks, without the need for a computer, micro-controller, or other programming source.

1. Introduction

High precision, extremely stable crystal oscillators are readily available at frequencies to around 150 MHz. Higher frequency sources, however, pose a much more difficult design challenge. Although it is possible to use overtones of inverted mesa crystal elements to reach oscillator frequencies above 600 MHz, these circuits are difficult to design and manufacture. A more common scheme for a high frequency, low jitter source is the Phase Locked Loop (PLL). The PLL transfers the excellent stability of a low frequency crystal source to arbitrarily high output frequencies. Figure 1 shows a typical block diagram of a PLL integrated system clock:

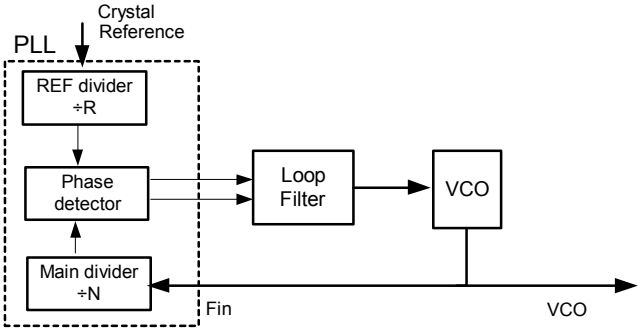

Figure 1. Block Diagram of PLL Integrated System Clock

In a PLL device, programmable counters divide the crystal reference and VCO (voltage controlled oscillator) inputs by the integer values R and N. A phase-frequency detector compares these two resultant signals and creates an error signal representing their frequency or phase difference. The VCO is then steered by this error signal until the loop is locked and the signals have identical frequency and phase. The VCO frequency at which that occurs is a factor N higher than the phase comparator frequency, and a factor $^{N}/_{R}$ higher than the crystal reference frequency. By choosing the appropriate crystal frequency and divider ratios, a designer can create any VCO frequency supported by the PLL.

2. Clock Design Considerations

Proper VCO choice is important for attaining good jitter performance. Lower tuning sensitivity generally yields better jitter, at the expense of tune range. A VCXO (voltage controlled crystal oscillator) is the best choice for clocks up to about 200 MHz. For higher frequencies (up to 1 GHz) a SAW device is often used in the resonant circuit instead of a crystal. Both VCXO and VCSO oscillator types deliver very low jitter but have narrow tuning ranges, typically 100 to 500 ppm/V. Above 1 GHz an L-C resonator is usually used, with a higher tuning sensitivity than a crystal or SAW oscillator.

Like any control system, the PLL has a loop bandwidth, i.e. a frequency range over which the output tracks the input. Optimizing the loop filter bandwidth is critical; this allows the lowest phase noise and jitter for a given set of components.

Within the loop bandwidth, the phase detector forces the VCO to track the reference, mapping the reference's phase noise onto the VCO. This process, however, is almost always dominated by the noise floor of the phase detector, which is usually higher than the reference oscillator noise profile. For offset frequencies greater than the loop bandwidth, the loop does not track the reference and the overall phase noise equals the VCO phase noise. The designer's task is to set the loop bandwidth to the point where the phase detector's noise floor intersects the VCO or VCXO (hereafter just VCO) free-running phase noise. Less bandwidth than this and the PLL can still improve the VCO phase noise; more than this and the PLL now begins to degrade the VCO phase noise.

Figure 2 illustrates phase noise profiles for loop filters that are too narrow, too wide, and optimum. The top solid black trace is the phase noise of a free-running VCO. It exhibits very poor phase noise near the carrier, improving rapidly at 30 dB per decade with increasing offset. At an inflection point, called the oscillator flicker corner, the downward slope transitions to 20 dB per decade. Eventually, the noise flattens at some very low floor limited by the oscillator's active devices.

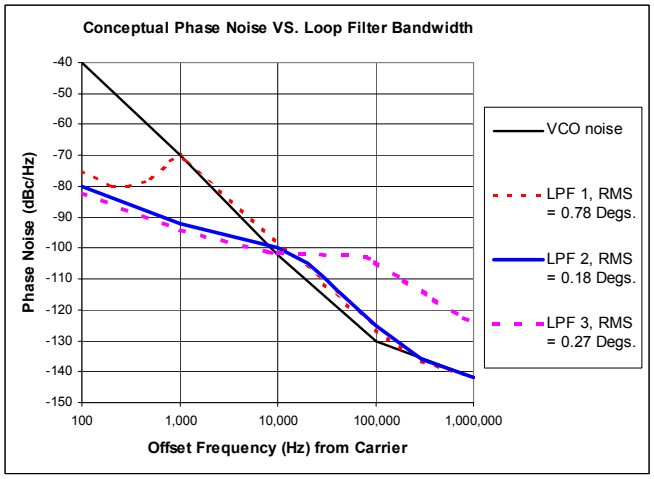

Figure 2. Conceptual phase noise of VCO/VCXO and PLL with various loop filter bandwidths

The ideal loop bandwidth is set where the PLL noise is equal to the VCO free-running noise. LPF #2 (the solid blue thick trace of Figure 2) illustrates this optimal solution. The phase noise with this design is relatively flat from the carrier to the corner frequency. There is little or no peaking at the corner, and beyond this point the noise follows the VCO noise characteristic.

If the loop bandwidth is narrower than the ideal (the trace labeled LPF #1 in Figure 2), large peaking appears at the corner frequency. The VCO noise is much worse than the phase detector noise at this frequency offset. The RMS jitter with LPF #1 will be higher than that with LPF #2.

On the other hand, if the loop bandwidth is wider than ideal (shown in the trace labeled LPF #3 in Figure 2) the phase detector noise is extended, dominating the better VCO free-running noise. The RMS jitter with the LPF #3 will also be higher than that with LPF #2 because the phase noise remains unnecessarily high beyond the optimum noise transition point.

One last consideration is the choice of R and N. A theoretically infinite number of values could be chosen that give the same final VCO frequency, and most PLLs support at least several realizable values. The best choice is the one that minimizes N, resulting in the highest possible comparison frequency. This minimizes the phase detector noise contribution, because any perturbation at the phase detector input (including its own noise, referred to its input) is magnified by the multiplication factor N before mapping to the VCO spectrum.

3. 155 MHz Clock Design and Performance

Each of the four test circuits evaluated implement the Figure 1 block diagram, and use an active loop filter as shown in Figure 3. Proper placement of the loop corner minimizes the overall output noise.

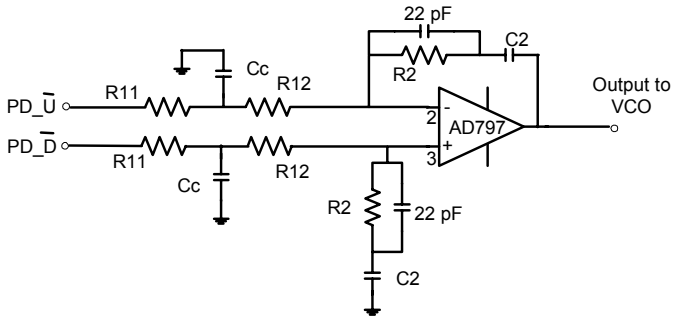

Figure 3. Loop Filter Configuration (see Table 3 for component values)

The first circuit uses a PE3236 PLL chip with a Vectron International (VI) VS-500A 155.52 MHz voltage-controlled SAW oscillator (VCSO). Figure 4 shows the phase noise and the RMS jitter spanning a 100 Hz to 1 MHz offset with various loop filter bandwidths. Although this VCSO nominally operates at the 155.52 MHz SONET OC-3 rate, a 155.625 MHz output frequency was chosen since it is derivable from a 10 MHz reference (the reference output from an Agilent 8561E Spectrum Analyzer). Loop performance was measured at bandwidths of 2.2, 3.3, 5.0, and 7.5 kHz.

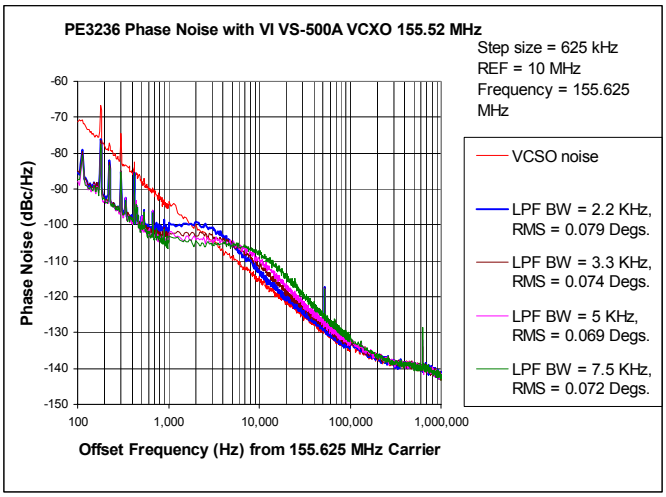

Figure 4. Phase Noise at Various Loop Bandwidths

LPF BW (kHz)	RMS noise* (Degrees)	RMS Jitter* (UI)	RMS Jitter* (ps)
2.2	0.079	0.000219	1.41
3.3	0.074	0.000205	1.32
5.0	0.069	0.000191	1.23
7.5	0.072	0.000200	1.29

**From 100 Hz to 1 MHz offset*
RMS Jitter (UI) = RMS noise° / 360°
RMS Jitter (Time) = RMS Jitter (UI) x Clock Period

Table 1. RMS noise and Jitter of PE3236 and VS-500A VCSO-155.52 MHz System

Table 1 lists the RMS phase noise and jitter of this circuit, integrated from 100 Hz to 1 MHz. The RMS phase noise ranged from 0.069 to 0.079 degrees, while the RMS time jitter spanned 1.23 to 1.41 ps. A 5.0 kHz loop bandwidth provided the lowest RMS phase noise.

4. Additional Clock Circuit Results

The PE3236 PLL integrated clock source was optimized for three other oscillators. The remaining VCSO example used the Vectron International VS-500A series at 622.08 MHz, while the two VCO examples used the MuRata MQE 744-450 and the Watkins-Johnson V1802-800. Figures 5, 6, and 7 show the overall phase noise of these three systems. Table 2 lists the integrated RMS noise and jitter measured for each system over a 100 Hz to 1 MHz offset. Refer to Table 3 oscillator tuning sensitivity, optimized loop filter bandwidth, and loop filter component values.

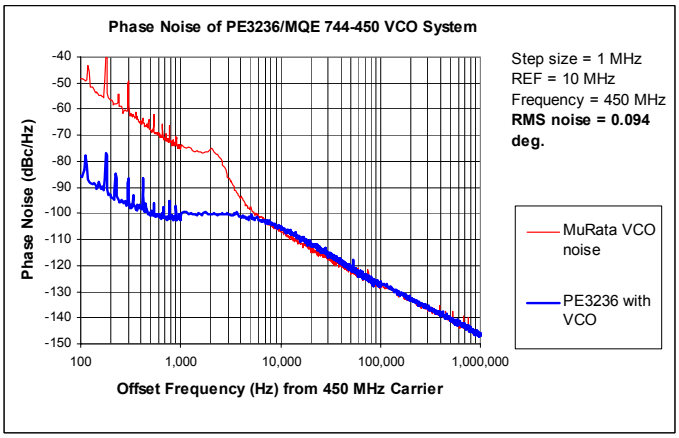

Figure 5. Phase Noise of PE3236 and MuRata MQE 744-450 VCO System

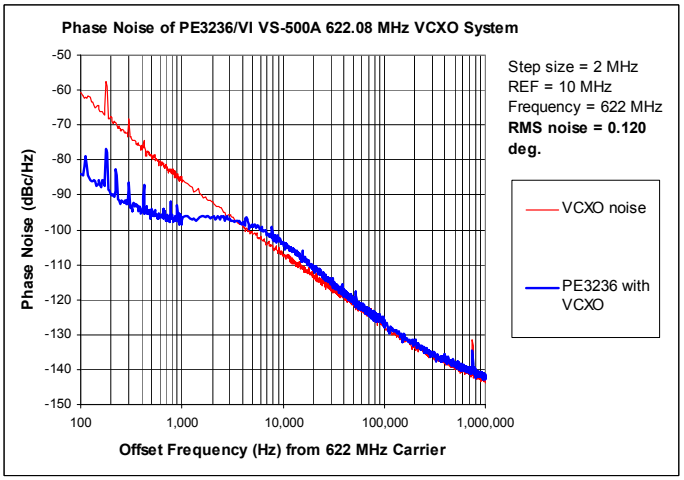

Figure 6. Phase Noise of PE3236 and VS-500A VCSO-622.08MHz System

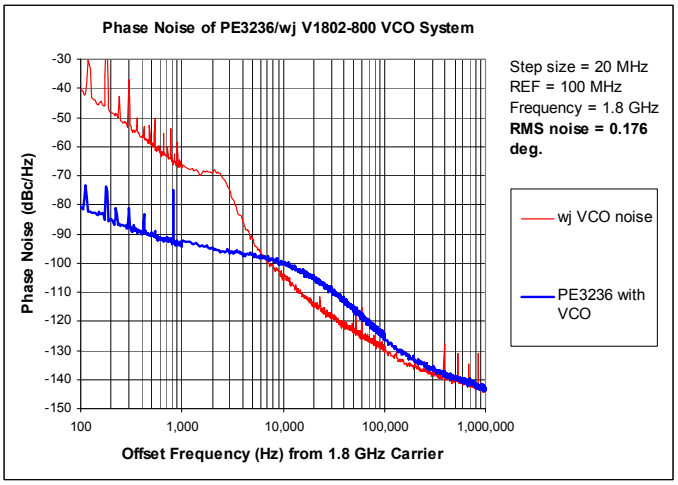

Figure 7. Phase Noise of PE3236/WJ VCO System

VCO	Freq. (MHz)	Period (ns)	RMS noise* (Degs)	RMS Jitter* (UI)	RMS Jitter* (ps)
VI VS-500A 155.52 MHz	155.625	6.43	0.069	1.917E-04	1.23
MuRata MQE 744-450	450	2.22	0.094	2.611E-04	0.58
VI VS-500A 622.08 MHz	622	1.61	0.12	3.333E-04	0.54
WJ V1802-800	1800	0.56	0.176	4.889E-04	0.27

**From 100 Hz to 1 MHz.*

RMS Jitter (UI) = RMS noise° / 360°

RMS Jitter (Time) = RMS Jitter (UI) X Clock Period (Time)

Table 2. Measured RMS noise and jitter of each PLL/VCXO or VCO system

						Loop Filter Components				
VCO	Kvco* (MHz/V)	VCO freq.* (MHz)	REF freq. (MHz)	Fc (MHz)	LPF BW (kHz)	R11 (W)	R12 (W)	R2 (W)	Cc (nF)	C2 (nF)
VI** VS-500A 155.52 MHz	0.0544	155.625	10	0.625	5.0	100	180	15K	100	10
MuRata MQE 744-450	3.91	450	10	5.0	7.5	390	470	330	22	300
VI** VS-500A 622.08 MHz	0.155	622	10	2.0	6.5	82	100	5.6K	112	22
WJ*** V1802-800	11.3	1800	100	33.33	15	390	470	150	10	360

Table 3. Center frequency, tuning gain, and optimized loop filter bandwidth and component values

**Note: The sensitivity Kvco was the actual measured value at the designated frequency. It might differ from the specified value of that VCSO or VCO. **VI = Vectron International ***WJ = WJ Communications*

5. Conclusion

The Peregrine Semiconductor PE3236 PLL combined with a low noise VCXO or VCO provides a very low jitter system clock. This report describes four examples with integrated RMS jitter over a 100 Hz to 1 MHz offset as low as 1.23, 0.58, 0.54 and 0.27 ps at frequencies of 155.625, 450, 622 and 1800 MHz, respectively.

Peregrine Semiconductor offers many other PLL and prescaler components that can be used in low jitter clock designs. For instance, the PE3336 extends frequency operation to 3 GHz. The PE3335 also operates to 3 GHz, and adds an on-chip charge pump that allows a passive loop filter to be used (no operational amplifier is required). Both versions are available in extremely small 7x7 MLP packages.

Peregrine PE3335 and PE3336 evaluation kits (part numbers 3335-01 and 3336-01) are available for rapid prototyping of the circuits described in this application note. The 7x7 MLP package versions of the PLLs supplied in these kits are ideally suited for space-conscious designs. In addition, both devices comes with a hardwire interface, ideal for fixed frequency applications where microcontrollers are not available.

Please visit our web site to find the best part for your application (www.peregrine-semi.com). All our current product data sheets are available, as well as application notes and software tools to assist in PLL loop filter design.

6. Acknowledgement

Thanks to Vectron International (www.vectron.com) for providing the VS-500 family VCSO samples used in this report.

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Application Note Identification

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